A Design of Ultra-Low Power Flip-Flop using Dual Change-Sensing Scheme

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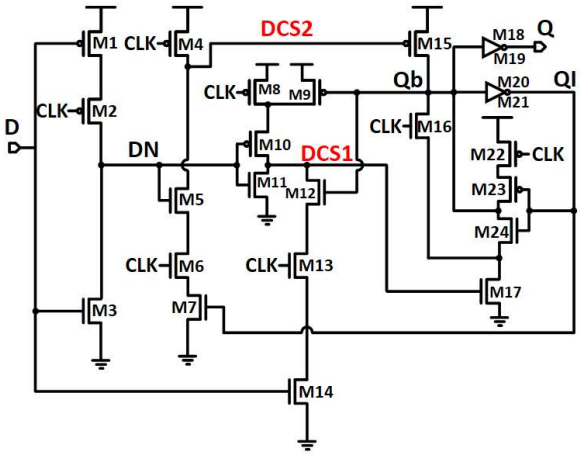
➢ Design Target

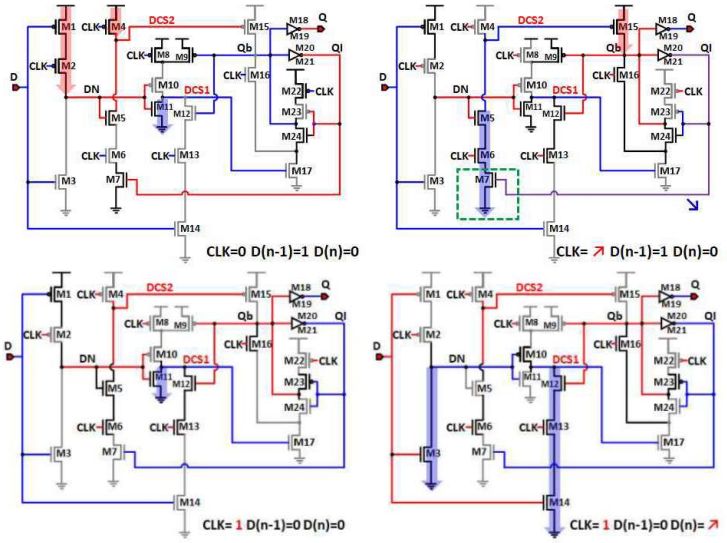
- Recently, research has been active in reducing power consumption as interest and demand for mobile system-on-chip (SoC) with limited energy consumption has increased.
- The limited energy consumption in SoC can be optimized by reducing the power consumption of flip-flops, the main component of SoC.
- The purpose of this study is to design flip-flop with low power consumption even at high data activity.

➢ Proposed DCSFF structure

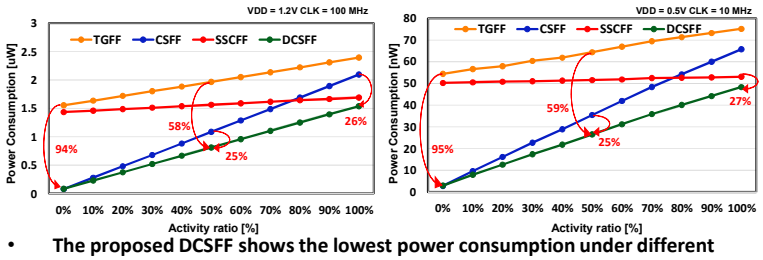


- The proposed DCSFF has low-power consumption even in high data activity ratio.

➢ Operation of proposed DCSFF

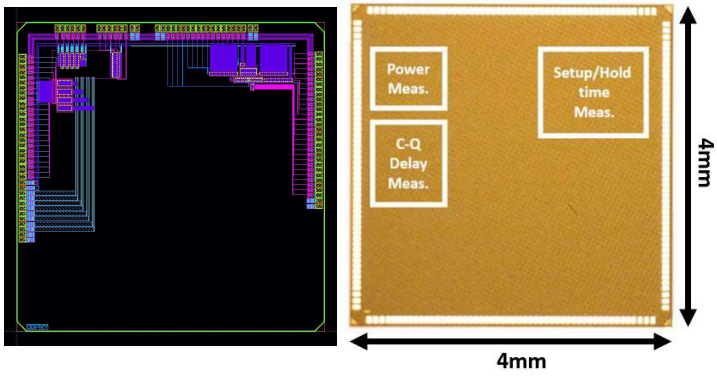


➢ Measurement results



- The proposed DCSFF shows the lowest power consumption under different conditions.

➢ Layout & Chip micrograph



- The manufactured chip consists of a DUT array and measurement block.

➢ Comparison table

	DCSFF (This work)	TGFF Conventional	S²CFF ISSCC' 14	CSFF JSSC' 18
Contention-Free	YES	YES	YES	NO
Number of Transistor	24	24	24	24
Single Phase Clock	YES	NO	YES	YES
Normalized Layout Size[A.U]	1.04	1	1.05	1.13
Measured C-Q Delay @1.2V	122.7 ps	150.6 ps	140.6 ps	128.9 ps
Measured Setup Time @1.2V	216 ps	165 ps	186 ps	197 ps
Measured Hold Time @1.2V	-46 ps	-34 ps	-49 ps	-55 ps
Measured Total Power @1.2V, 100MHz, 20% Activity	0.37 μW	1.72 μW	1.49 μW	0.48μW
Measured Total Power @0.5V, 10MHz, 20% Activity	12.6 nW	57.9 nW	50.8 nW	16.2 nW
Measured Total Power @1.2V, 100MHz, 100% Activity	1.54 μW	2.39 μW	1.69 μW	2.09 μW
Measured Total Power @0.5V, 10MHz, 100% Activity	48.3 nW	75.2 nW	53.1 nW	65.8 nW
Measured Leakage @1.2V	0.084 μW	1.555 μW	1.435 μW	0.079 μW

➢ Summary

- The proposed flip-flop can optimize glitch, short circuit current to reduce power consumption.
- The purpose of the study is the design of flip-flop, which has low-power consumption even at high data activity.